ATC Card Design Issues

Johnny Green
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Introduction

The purpose of this document is to explain the how and why the ATC printed circuit board designed and later required a revision.
The ATC (ADF Transition card) is a 6U x 220mm x 0.093, 8 layer, with all layers of one ounce copper. These VME64 Transition boards used with ADF (Analog Digital Filter) module are part of the L1-Cal Trigger upgrade. There are a total of 80 ADF modules that are housed in 4- VME64 crates. Each ADF requires one ATC to transition to other subsystems.
The ATC was developed as a passive bus extender for interfacing LVDS and analog signals to the ADF modules. The ATC wiring is critical to the performance of the ADF module so close detail was paid to the design. It was determined that the best method for matching the ADF/ATC to other subsystem was to use differential-mode characteristic impedances of strip-lines.
The broadside –coupled strip-line design was chosen for this purpose.
The board is separated into two halves. The upper half of the board is used for the LVDS circuits has a Z of 100 ohms. The lower half of the board is used for analog circuits has a Z of 72 ohms.
The first design of the board was considered to be adequate. After receiving the boards several were stuffed. Later it found that the bow of the boards was the issue to their implementation. It was first thought that the bowing might be related to the construction techniques of the board house, so a specification was given for flatness that they had to meet.
After some numerous tries the board house returned to us and explained that they could not build the board as designed. They informed us that they thought the bowing problem was due to thermal effects of the layer stacking.
Figure 1 shows the layer stacking as designed initially. As you will notice the board was designed as a controlled impedance broadside coupled strip line circuit. The top layer had no copper. The controlled impedance Layers 2,3,4 & 5 form one set of broadside-coupled strip-lines. The return plane on layer 5 is re-used to create a second set of broadside-coupled strip-lines on layers 5,6,7 & 8

The issues related to layer stacking symmetry are concerning thermal expansion and cooling of the printed circuit board during its manufacture.

First Design Description

There are 3 ground planes in the first design layered fairly close to a symmetrical cross section. The issue with this scheme is that layer 2 which is insulated by layer 1 will cool at a slower rate than layer 8. It is possible that a cooling differential might occur which could cause bowing.
There were 25 boards made using the first design before the problem of bowing was discovered. Of the boards built only 10 were judged flat enough to be used in the ADF crate.

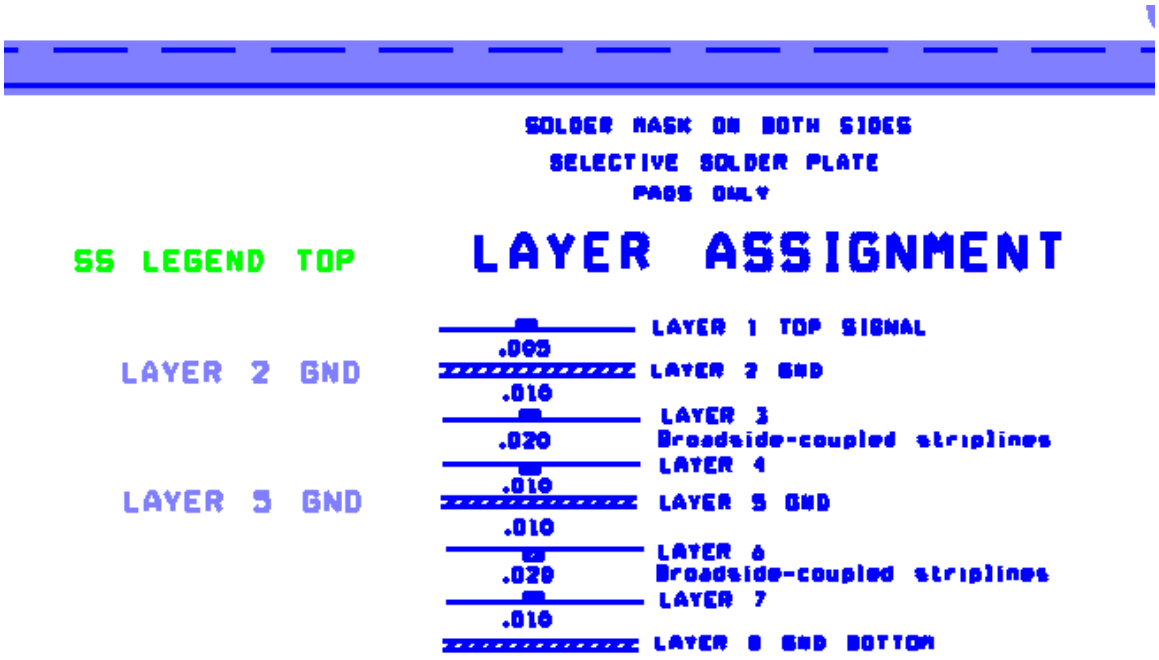

Figure 1.

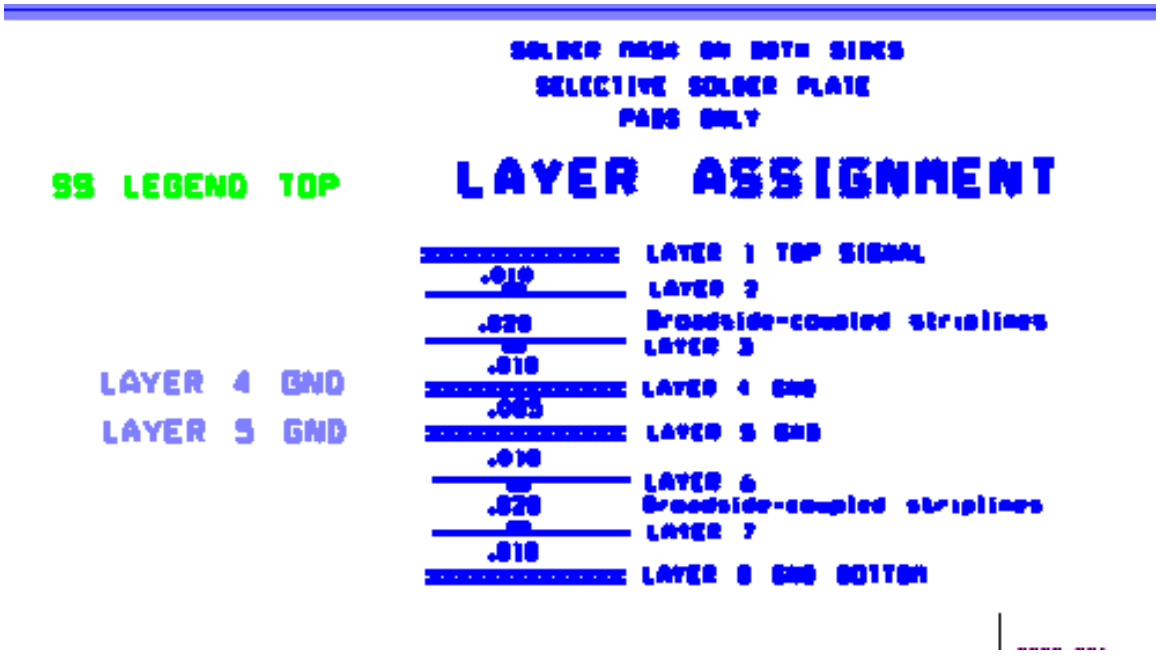

Figure 2

Revised Design

The revised layer stacking is much improved in the sense of symmetry. Both layer 1 and layer 8 have the same mass, which should give the same rate of cooling. See Figure 2. There is now an even number of plane layers, which are spaced equally in the stacking. The board cross sections are now an exact mirror images, so it follows the characteristics should also be the same.

The spacing of layers 1,2,3,4 and layers 5,6,7,8 will have the same differential-mode characteristic impedances as the first design.

Other Factors

The board house has many options as to ways that they can build the board. Typically, they will start with the thickest materials to the inside and build to the outside with the thinner materials. Layer thicknesses are built from standard cores available commercially. Standard core thicknesses for ML PCBs: 5, 8, 10, 14, 20, 40 mil. Prepreg thicknesses are 4mil typically. If the board house is not diligent and the dielectric grains are not in the same direction, or the Core or Prepreg material has a tendency to bow, or the material is old, or the wrong type, bow can occur. I've been told that extending the cool down period while the board is under pressure will aid in making sure that any internal stresses will be relieved, can aid in board flatness.

Conclusion:

We are concerned that thermal effects cannot explain the total reason for the bow primarily because some of the boards that we received were bowed in opposite directions. The thermal effects are but one factor that might have influenced the bow.

It is our expectation that the revised layer stacking will significantly reduce the possibility of any bowing due to thermal effects. We expect that there will be no change in electrical performance of this board. We expect that our board house has now determined all the other factors relating to the build so that we will receive boards that will meet the IPC specification of 7mil/linear inch maximum bow.